CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus;

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus; and

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

2. The integrated circuit of claim 1, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

3. The integrated circuit of claim 1, wherein the microcontroller is configured as an Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

4. The integrated circuit of claim 1, wherein the microcontroller is configured as an Alert Standard Format slave, and wherein the Ethernet controller is configured to route Alert Standard Format messages to an external Alert Standard Format master.

5. The integrated circuit of claim 1, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

6. The integrated circuit of claim 1, further comprising:

a status register configured to store Alert Standard Format sensor data, wherein the Alert Standard Format sensor data is stored in the status register by the microcontroller.

7. The integrated circuit of claim 6, further comprising:

a power port configured to receive a reserve power signal, wherein the reserve power signal provides reserve power to the status register configured to store Alert Standard Format sensor data.

8. The integrated circuit of claim 1, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

9. The bridge of claim 8, wherein the bridge is configured as a south bridge.

10. The south bridge of claim 9, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bridge.

11. The integrated circuit of claim 1, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured

to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

12. The integrated circuit of claim 1, further comprising:

a memory connected to the internal bus.

13. The integrated circuit of claim 12, wherein the memory includes a read-only memory.

14. The integrated circuit of claim 12, wherein the memory includes random access memory.

15. The integrated circuit of claim 14, wherein the random access memory is configured to shadow a read-only memory.

16. The integrated circuit of claim 14, wherein the random access memory is loaded during a boot-up process.

17. The integrated circuit of claim 1, wherein the microcontroller is configured to manage security in a computer system.

18. The integrated circuit of claim 1, wherein the microcontroller is configured to manage health status of a computer system.

19. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus; and

a system management interrupt request register coupled to the internal bus, wherein the system management interrupt request register is configured to generate a request for a system management interrupt in response to a system management interrupt vector written to the system management interrupt request register, wherein the microcontroller is configured to write the system management interrupt vector to the system management interrupt request register.

20. The integrated circuit of claim 19, further comprising:

a timer coupled to the internal bus, wherein the microcontroller is configurable to write the system management interrupt vector to the system management interrupt request register in response to an expiration of the timer.

21. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus; and

an interrupt register coupled to the internal bus, wherein a microcontroller interrupt is generated in response to a microcontroller interrupt vector written to the interrupt register.

22. The integrated circuit of claim 21, further comprising:

a data exchange register coupled to the internal bus, wherein the data exchange register is configured to store data from the microcontroller or for the microcontroller, wherein the microcontroller is configured to write data to the data exchange register, and wherein the microcontroller is configured to read data from the data exchange register.

23. The integrated circuit of claim 21, further comprising:

a system management interrupt request register coupled to the internal bus, wherein the system management interrupt request register is configured to generate a request for a system management interrupt in response to a system management interrupt vector written to the system management interrupt request register, wherein the microcontroller is configured to write the system management interrupt vector to the system management interrupt request register.

24. An integrated circuit, comprising:

an internal bus;

means for processing coupled to the internal bus, wherein the means for processing are configured to master the internal bus;

means for networking coupled to the internal bus, wherein the means for networking and the means for processing exchange data over the internal bus; and

a plurality of storage means coupled between the means for processing and the means for networking for buffering the data.

25. The integrated circuit of claim 24, wherein the means for processing are configured as an Alert Standard Format master, and wherein the means for networking is configured to route Alert Standard Format messages to the means for processing.

26. The integrated circuit of claim 24, wherein the means for processing is configured as an Alert Standard Format slave, and wherein the means for networking is configured to route Alert Standard Format messages to an external Alert Standard Format master.

27. The integrated circuit of claim 24, further comprising:

means for execute remote management and control protocol commands received from an external management server through the means for networking.

28. The integrated circuit of claim 24, further comprising:

means for managing security in a computer system.

29. The integrated circuit of claim 24, further comprising:

means for managing health status of a computer system.

30. An integrated circuit, comprising:

an internal bus;

means for processing connected to the internal bus, wherein the means for processing are configured to master the internal bus; and

means for generating a system management interrupt coupled to the internal bus, wherein the means for processing are configured to activate the means for generating a system management interrupt.

31. An integrated circuit, comprising:

an internal bus;

means for processing coupled to the internal bus, wherein the means for processing are configured to master the internal bus; and

means for generating an interrupt to the means for processing, wherein an interrupt is generated to the means for processing.

32. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus;

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus;

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus, wherein the processor is configured to communicate over a network using the Ethernet controller.

33. The computer system of claim 32, wherein the microcontroller is configured as an Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

34. The computer system of claim 32, further comprising:

a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as an Alert Standard Format master, wherein the microcontroller is configured as an Alert Standard Format slave, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card.

35. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus;

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus;

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data; and

a bus interface logic connected to the external bus; and

one or more sensors coupled to the external bus, wherein the Ethernet controller is configured to transmit data from the sensors over a network.

36. The computer system of claim 35, wherein the microcontroller is configured as an Alert Standard Format master, and wherein the Ethernet controller is configured to route

Alert Standard Format messages to the microcontroller, and wherein the microcontroller is configured to poll the sensors over the external bus.

37. The computer system of claim 35, wherein the microcontroller is configured to manage security in the computer system.

38. The computer system of claim 35, wherein the microcontroller is configured to manage health status of the computer system.

39. The computer system of claim 35, further comprising:

a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as an Alert Standard Format master, wherein the network interface card is configured to poll the sensors over the external bus, wherein the microcontroller is configured as an Alert Standard Format slave, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card.

40. A method for operating a computer system, the method comprising:

receiving a Alert Standard Format message at a Ethernet controller in an Alert Standard Format south bridge;

transmitting the Alert Standard Format message from the Ethernet controller in the Alert Standard Format south bridge to a microcontroller in the Alert Standard Format south bridge over an internal bus in the Alert Standard Format south bridge;

when operating the microcontroller in the Alert Standard Format south bridge in an Alert Standard Format slave mode, transmitting the Alert Standard Format message from

the microcontroller in the Alert Standard Format south bridge over an external bus to an the Alert Standard Format network interface card; and

when operating the microcontroller in the Alert Standard Format south bridge in an Alert Standard Format master mode, sending an acknowledgement to the Alert Standard Format message from the microcontroller in the Alert Standard Format south bridge to the Ethernet controller in the Alert Standard Format south bridge.

41. The method of claim 40, further comprising:

reading data from one or more of a plurality of Alert Standard Format south bridge registers in response to the Alert Standard Format message.

42. The method of claim 41, further comprising:

when operating the microcontroller in the Alert Standard Format south bridge in the Alert Standard Format slave mode, then transferring the data from the one or more of the plurality of Alert Standard Format south bridge registers from the network interface card to the microcontroller in the Alert Standard Format south bridge over the external bus; and

transferring the data from the one or more of the plurality of Alert Standard Format south bridge registers from the microcontroller in the Alert Standard Format south bridge to the Ethernet controller in the Alert Standard Format south bridge over the internal bridge.

43. The method of claim 41, wherein operating the microcontroller in the Alert Standard Format south bridge in the Alert Standard Format master mode comprises microcontroller in the Alert Standard Format south bridge polling Alert Standard

Format sensors in the computer system for Alert Standard Format sensor status values and responding to requests from an external management server for the Alert Standard Format sensor status values.

44. The method of claim 41, wherein operating the microcontroller in the Alert Standard Format south bridge in the Alert Standard Format slave mode comprises responding to Alert Standard Format requests from the Alert Standard Format network interface card by the microcontroller in the Alert Standard Format south bridge.

.45. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving a Alert Standard Format message at a Ethernet controller in an Alert Standard Format south bridge;

transmitting the Alert Standard Format message from the Ethernet controller in the Alert Standard Format south bridge to a microcontroller in the Alert Standard Format south bridge over an internal bus in the Alert Standard Format south bridge;

when operating the microcontroller in the Alert Standard Format south bridge in an Alert Standard Format slave mode, transmitting the Alert Standard Format message from the microcontroller in the Alert Standard Format south bridge over an external bus to an the Alert Standard Format network interface card; and

when operating the microcontroller in the Alert Standard Format south bridge in an Alert Standard Format master mode, sending an acknowledgement to the Alert Standard Format message from the microcontroller in the Alert Standard Format south bridge to the Ethernet controller in the Alert Standard Format south bridge.

46. The computer readable medium as set forth in claim 45, the method further comprising:

reading data from one or more of a plurality of Alert Standard Format south bridge registers in response to the Alert Standard Format message.

47. The computer readable medium as set forth in claim 46, wherein operating the microcontroller in the Alert Standard Format south bridge in the Alert Standard Format master mode comprises microcontroller in the Alert Standard Format south bridge polling Alert Standard Format sensors in the computer system for Alert Standard Format sensor status values and responding to requests from an external management server for the Alert Standard Format sensor status values.

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~~47.~~ The computer readable medium as set forth in claim 46, wherein operating the microcontroller in the Alert Standard Format south bridge in the Alert Standard Format slave mode comprises responding to Alert Standard Format requests from the Alert Standard Format network interface card by the microcontroller in the Alert Standard Format south bridge.